

LNK454/456-458/460

LinkSwitch-PL Family



LED Driver IC with TRIAC Dimming, Single-Stage PFC and Constant Current Control for Non-Isolated Applications

Product Highlights

Dramatically Simplifies Off-line LED Drivers

- Single stage power factor correction and accurate constant current (CC) output
- Flicker-free phase-controlled TRIAC dimming
- Very low component count with small non-electrolytic bulk capacitor, for compact replacement lamp designs
- Compact SO8 package
- Completely eliminates control loop compensation

Advanced Performance Features

- Optimized for non-isolated flyback designs
- Frequency jitter greatly reduces EMI filter size and costs
- Low dissipation direct sensing of LED current

Advanced Protection and Safety Features

- 725 V integrated MOSFET allows small bulk capacitance and maximizes power capability
- Latching shutdown protection for short-circuit / open feedback and output overvoltage
- Auto-restart for overload condition
- Hysteretic thermal shutdown
- Meets high-voltage creepage between DRAIN and all other pins both on PCB and at package

EcoSmart® - Energy Efficient

- High power factor optimizes system lumen per watt by reducing input VA
- Control algorithm balances switching and conduction losses over line and load to maintain optimum efficiency
- Cycle skipping regulation for abnormally low output power to clamp peak output current delivered

Description

The LinkSwitch-PL family enables a very small and low cost single-stage power factor corrected constant current driver for solid state lighting. Optimized for direct LED current sensing, the LinkSwitch-PL operates over a wide input voltage range delivering an output power of up to 16 W. The LinkSwitch-PL control algorithm provides flicker-free TRIAC dimming with minimal external components.

Each device incorporates a 725 V rated power MOSFET, a novel discontinuous mode variable frequency variable on-time controller, frequency jitter, cycle by cycle current limit and hysteretic thermal shutdown in a monolithic 4-pin IC, available in SO-8C and eDIP-12 packages.

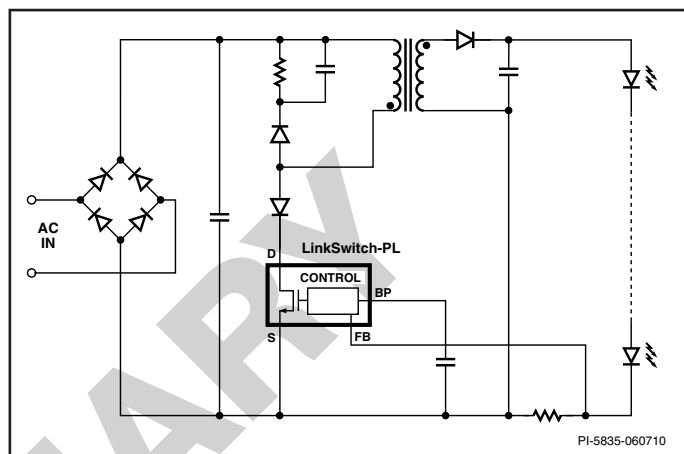


Figure 1. Basic Application Schematic.

Output Power Table

Product ²	85-265 VAC	
	Minimum Output Power ¹	Maximum Output Power ¹
LNK454D	1.5 W	3 W
LNK456D	3 W	6 W
LNK457D/V	4 W	8 W
LNK458V	6 W	11.5 W
LNK460V	8 W	16 W

Table 1. Output Power Table.

Notes:

1. Maximum practical continuous power in an open frame design with adequate heat sinking, measured at +50 °C ambient (see Key Applications Considerations for more information).
2. Packages: D: SO-8C, V: eDIP-12.

Number of Serial LEDs	Output Current			
	350 mA	500 mA	700 mA	1000 mA
1	LNK454	LNK454	LNK454	LNK456
2	LNK454	LNK456	LNK456	LNK457
3	LNK456	LNK456	LNK457	LNK458
4	LNK456	LNK457	LNK458	LNK460
5	LNK457	LNK458	LNK460	
6	LNK457	LNK458	LNK460	
7	LNK458	LNK460		
8	LNK458	LNK460		
9	LNK458	LNK460		
10	LNK460			
11	LNK460			
12	LNK460			

Figure 2. Device Selection based on Length of Output LED Series String and Current. A Typical Voltage Drop of 3.5 V per LED is Assumed.

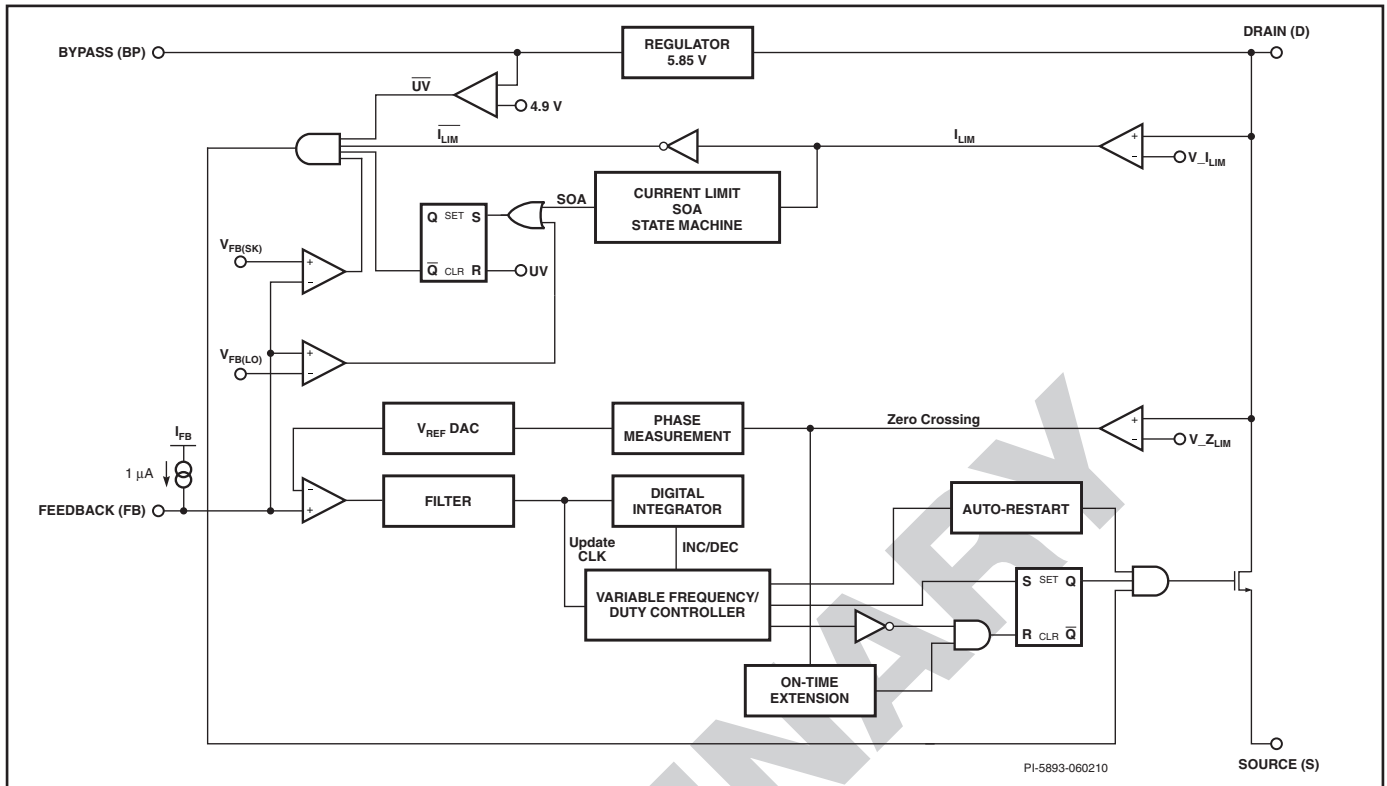


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:

High-voltage power MOSFET drain connection. The internal start-up bias current is drawn from this pin through a switched high-voltage current source. Drain current sensing and associated controller functions are also performed using this pin.

SOURCE (S) Pin:

Power MOSFET source connection. Ground reference for BYPASS and FEEDBACK pins.

BYPASS (BP) Pin:

Connection point for the external bypass capacitor for the internally generated 5.85 V supply.

FEEDBACK (FB) Pin:

LED current sensing pin. During normal operation the 290 mV threshold determines the average value of the current flowing through the load sense resistor.

A second higher threshold clamps excessive output current ripple.

An additional higher threshold is used to protect against output short-circuit and overvoltage conditions.

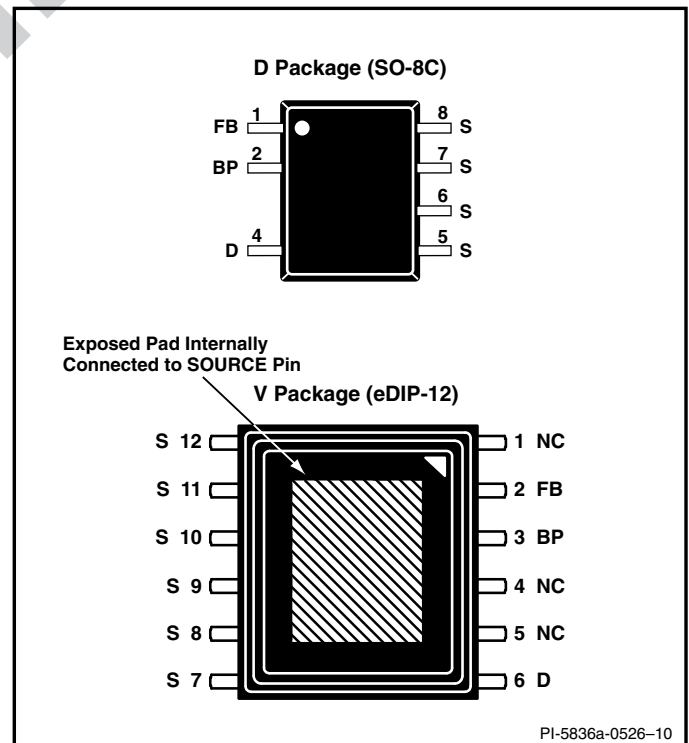


Figure 3. Pin Configuration (Top View).

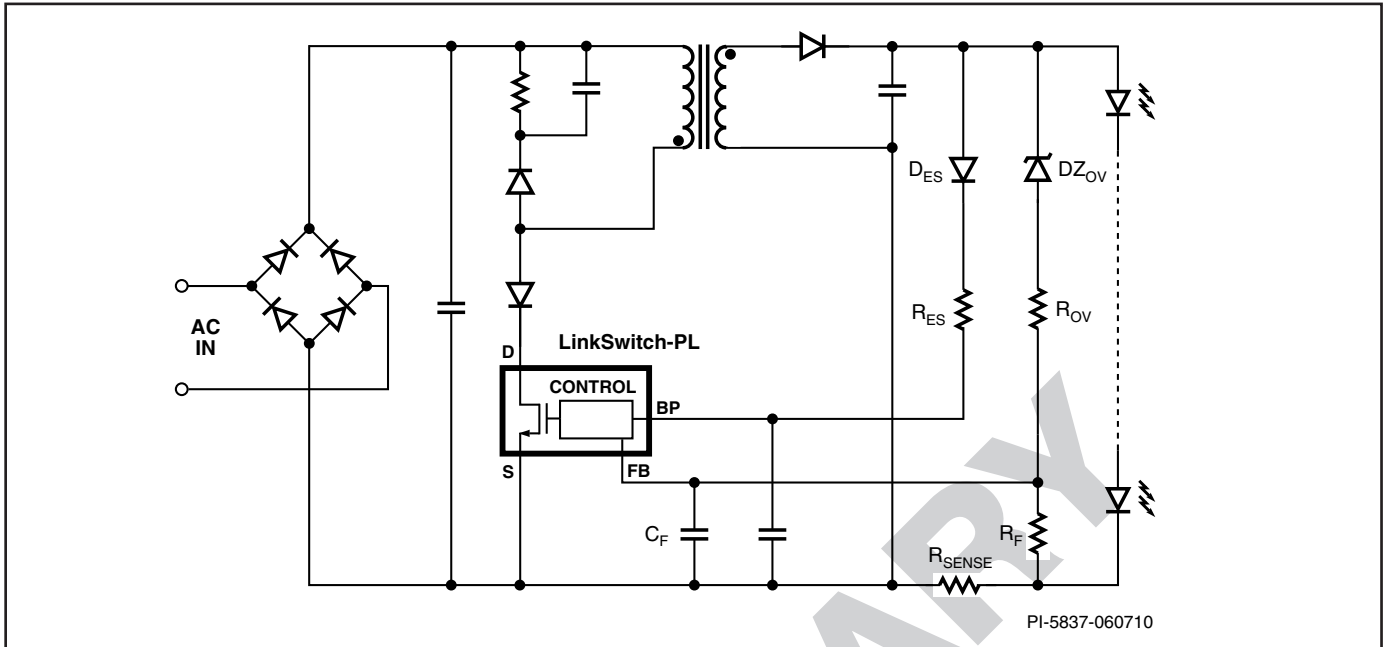


Figure 4. Typical Application Schematic.

Functional Description

The LinkSwitch-PL combines a high-voltage power MOSFET switch with a power supply controller in one device. The IC provides a single stage power factor correction plus LED current control. The LinkSwitch-PL controller consists of an oscillator, feedback (sense and logic) circuit, 5.85 V regulator, hysteretic over-temperature protection, frequency jittering, cycle-by-cycle current limit, loop compensation circuitry, auto-restart, switching on-time extension, power factor and constant current control.

In a direct LED current sensing configuration, the average FEEDBACK pin voltage is a replica of the LED current, scaled by the sense resistor (R_{SENSE} in Figure 4). A small low-pass filter (R_F and C_F in Figure 4) reduces high frequency noise at the FEEDBACK pin.

Figure 5 illustrates the operating regions of the FEEDBACK pin voltage. The LinkSwitch-PL sets its operating point such that the average FEEDBACK pin voltage in steady-state operation is 290 mV. This threshold is low to minimize the sensing resistor dissipation. The internal MOSFET switching frequency and on-time are updated once every input AC half-cycle to regulate the output current and maintain high power factor.

If the FEEDBACK pin peak voltage exceeds 520 mV, cycle skipping mode is triggered and the power processed by the integrated MOSFET is clamped on a cycle-by-cycle basis. Switching frequency may vary during an input voltage half-cycle to reduce thermal stress on the output LEDs.

Latching shutdown protection is triggered by a FEEDBACK pin voltage in excess of 2 V. This feature can be used to provide output overvoltage protection (via DZ_{OV} and R_{OV} in Figure 4), which triggers the IC to latch off. This condition is reset when the BYPASS pin voltage drops below 4.9 V, after removal of the AC input.

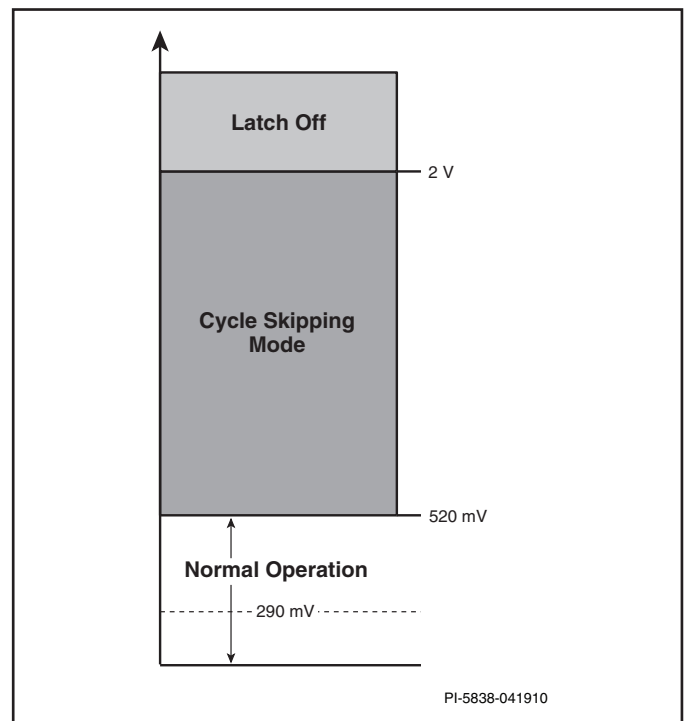


Figure 5. FEEDBACK Pin Operation Voltage Thresholds.

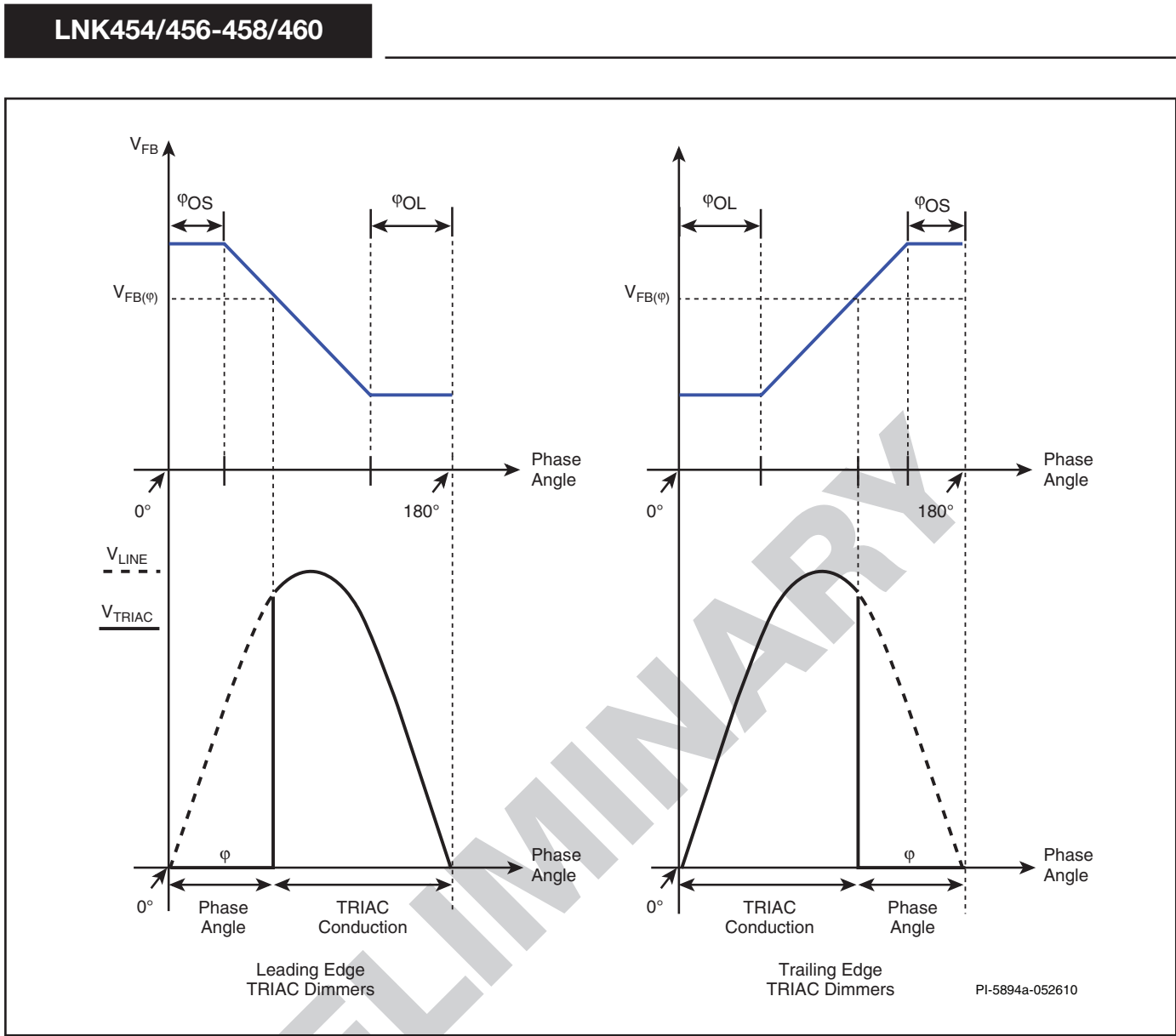


Figure 6. Feedback Voltage vs. Phase Angle Dimming Characteristics.

TRIAC (Phase-Controlled) Dimming

The LinkSwitch-PL integrates several features to improve dimming range and reduce external circuit complexity when using a phase-controlled TRIAC dimmer. The output LED current is controlled by the FEEDBACK pin voltage which changes proportionally to the TRIAC dimmer conduction angle. The conduction angle decreases, the voltage at the FEEDBACK pin decreases causing the average LED current to decrease.

The FEEDBACK pin voltage adjustment is initiated at approximately 20% of the main half-cycle duration. When this (ϕ_{OS}) threshold is exceeded, V_{FB} and the output LED current are reduced until a second phase angle threshold is reached. When this happens, with the TRIAC conduction angle being

very limited, the IC runs open loop (ϕ OL region) and the integrated MOSFET processes as much power as the heavily chopped input voltage will allow creating a light output that is deeply dimmed.

The 520 mV clamping feedback threshold is also linearly reduced during dimming to control LED current ripple.

To help maintain the holding current of the TRIAC in the dimmer, LinkSwitch-PL extends the MOSFET on-time towards the zero crossings of the AC input voltage providing an active bleed or holding current function. This on-time extension is carefully limited to avoid deterioration of input current harmonic content and limit total harmonic distortion (THD).

IC Supply and BYPASS Pin

The internal 5.85 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.85 V by drawing current from the voltage on the DRAIN pin whenever the power MOSFET is off. The BYPASS pin is the internal supply voltage node. When the power MOSFET is on, the device operates from the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows LinkSwitch-PL to operate continuously from current it takes from the DRAIN pin. A bypass capacitor value of 1 μ F is sufficient for both high frequency decoupling and energy storage.

During phase angle dimming when the conduction angle is small the AC input voltage is present for only short periods of time. In that case the IC should not rely on the integrated high voltage current source, but instead external bias circuitry should be used to supply the IC from the output (D_{ES} and R_{ES} in Figure 4). If the output voltage is less than 7 V, external bias circuitry should be implemented, by using a bias winding on the primary of the transformer with a small signal rectifier and an electrolytic capacitor with a value based on maximum IC consumption and maximum phase dimming conduction angles.

Start-up, Switching Frequency, On-time Range

At start-up the controller uses an initial switching frequency f_{MIN} and minimum on-time $t_{ON(MIN)}$. The charging of the output capacitor together with the energy delivery to the output LEDs as soon as their anode-cathode threshold is reached determines a step-by-step increase of the operating power MOSFET switching frequency and on-time every half-cycle of the main input voltage.

When the operating conditions (start-up or large transients) allow for only low energy processing (low frequency and on-time), the voltage across the input bulk capacitance will not reach zero even if the main voltage crosses zero. During these conditions the IC sets the reference voltage on the FEEDBACK pin to one half of its preset level (145 mV), to avoid overshoot of the output LED current. Once the FEEDBACK pin voltage exceeds this reduced threshold (with the zero crossing on the bulk capacitor being achieved), then the FEEDBACK pin voltage is restored to the normal 290 mV level.

The steady state switching frequency and on-time is determined by the line voltage, voltage drop across the LEDs and system overall power transfer efficiency.

At light load when the device reaches the minimum frequency f_{MIN} and on-time $t_{ON(MIN)}$, the controller regulates by skipping cycles. In this mode of operation the input current is not power factor corrected and the average output current is not guaranteed to fall within the normal range. The FEEDBACK pin cycle skipping threshold is reduced from approximately twice the normal regulation level down to just above the level required to limit output power delivery under these conditions. A

properly designed supply will not operate in this mode under normal load conditions. A power supply designed correctly will operate within the switching frequency range $[f_{MIN} \dots f_{MAX}]$, with an on-time falling between $t_{ON(MIN)}$ and $t_{ON(MAX)}$ when connected to a normal load.

Overload Protection

In case of overload, the system will increase the operating frequency and on-time each AC half-cycle until the maximum frequency and maximum on-time are reached. When this state is reached, by the next half-cycle, the controller will enter auto-restart protection, thus inhibiting the gate of the power MOSFET for approximately 1.28 s if the main line frequency is 50 Hz, 1.02 s if it is 60 Hz. After this auto-restart off-time expires, the circuit will start again, exactly as at start-up, i.e. at f_{MIN} and $t_{ON(MIN)}$, stepping up until regulation is achieved again. In case of a persistent overload condition, the auto-restart duty cycle DC_{AR} will typically be as low as 33%.

Auto-restart is inhibited during phase dimming when the TRIAC conduction duty cycle is less than 60%.

Output Overvoltage Protection

If a no-load condition is present on the output of the supply, the output overvoltage Zener (DZ_{OV} in Figure 4) will conduct once its threshold is reached. A voltage V_{OV} in excess of $V_{FB(LO)} = 2$ V will appear across the FEEDBACK pin and the IC will latch off. Normal operation will be restored once the BYPASS pin voltage drops below 4.9 V and the IC goes through a new start-up phase.

Output Short-Circuit

If the output of the supply (i.e. the LED load) is short-circuited, then a large amount of energy will be delivered to the sense resistor, generating a high voltage at the FEEDBACK pin. If this condition develops more than 2 V on the FEEDBACK pin, then the IC will interpret this event as an output short-circuit and will trigger latching shutdown. Normal operation will resume after cycling the AC input such that the BYPASS pin voltage drops below 4.9 V and the IC goes through a new start-up phase.

Safe Operating Area (SOA) Protection

If 3 consecutive cycles of the power MOSFET are prematurely terminated due to the power MOSFET current exceeding the current limit after the leading edge blanking time, SOA protection mode is triggered and the IC will trigger latching shutdown. Normal operation will resume after cycling the AC input such that the BYPASS pin voltage drops below 4.9 V and the IC goes through a new start-up phase.

Hysteretic Thermal Shutdown

The thermal shutdown circuitry senses the die junction temperature. The thermal shutdown threshold is set to 142 °C typical with a 75 °C hysteresis. When the die temperature rises above this threshold (142 °C) the power MOSFET is disabled and remains disabled until the die temperature falls by 75 °C, at which point the power MOSFET is re-enabled.

Absolute Maximum Ratings^(1,4)

DRAIN Pin Peak Current:	LNK454	400 mA (750 mA)
	LNK456	850 mA (1450 mA)
	LNK457	1350 mA (2000 mA)
	LNK458	1750 mA (2650 mA)
	LNK460	2700 mA (5100 mA)
DRAIN Pin Voltage		-0.3 V to 725 V
FEEDBACK Pin Voltage		-0.3 to 9 V
BYPASS Pin Voltage		-0.3 to 9 V
Lead Temperature ⁽³⁾		260 °C
Storage Temperature		-65 to 150 °C
Operating Junction Temperature ⁽²⁾		-40 to 150 °C

Notes:

1. All voltages referenced to SOURCE, $T_A = 25\text{ °C}$.
2. Normally limited by internal circuitry.
3. 1/16 in. from case for 5 seconds.
4. The Absolute Maximum Ratings specified may be applied, one at a time without causing permanent damage to the product. Exposure to Absolute Maximum Ratings for extended periods of time may affect product reliability.

Thermal Resistance

Thermal Resistance: D (SO-8C) Package:

(θ_{JA})	100 °C/W ⁽¹⁾ , 80 °C/W ⁽²⁾
(θ_{JC})	30 °C/W ⁽³⁾

V (eDIP) Package:

(θ_{JA})	68 °C/W ⁽¹⁾ , 58 °C/W ⁽²⁾
(θ_{JC})	2 °C/W ⁽⁴⁾

Notes:

1. Soldered to 0.36 sq. in. (232 mm²), 2 oz. (610g/m²) copper clad, with no external heat sink attached.
2. Soldered to 1 sq. in. (645 mm²), 2 oz. (610g/m²) copper clad, with no external heat sink attached.
3. Measured on the SOURCE pin close to plastic interface.
4. Measured at the surface of exposed pad.

Parameter	Symbol	Conditions SOURCE = 0 V; $T_J = -40$ to $+125\text{ °C}$ (Unless Otherwise Specified)	Min	Typ	Max	Units
Control Functions						
Maximum Output Frequency	f_{MAX}	$T_J = 25\text{ °C}$	Average	110	122	134 kHz
			Peak-Peak Jitter		6	%
Minimum Output Frequency	f_{MIN}	$T_J = 25\text{ °C}$	Average	25.8	28.7	31.6 kHz
			Peak-Peak Jitter		6	%
Maximum Switch ON-Time	$t_{ON(MAX)}$	$T_J = 25\text{ °C}$		5.74		μs
Minimum Switch ON-Time	$t_{ON(MIN)}$	$T_J = 25\text{ °C}$		1.18		μs
ON-Time Extension	t_{EXT}			5.2		μs
Maximum Duty Cycle	DC_{MAX}			70		%
FEEDBACK Pin Voltage	V_{FB}	$T_J = 25\text{ °C}$	275	290	305	mV
FEEDBACK Pin Voltage Triggering Cycle Skipping Mode	$V_{FB(SK)}$			520		mV
FEEDBACK Pin Voltage for IC Latch-OFF	$V_{FB(LO)}$			2000		mV
Feedback Pull-up Current	I_{FB}		-1.3	-1.0	-0.7	μA

Parameter	Symbol	Conditions SOURCE = 0 V; T _J = -40 to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Control Function (cont.)							
DRAIN Supply Current	I _{S1}	V _{FB} > V _{FB(SK)} (MOSFET not switching)			450		μA
	I _{S2}	V _{FB} = 0 V (MOSFET switching at f _{MAX})	LNK454		530		μA
			LNK456		585		
			LNK457		650		
			LNK458		730		
			LNK460		1050		
BYPASS Pin Charge Current	I _{CH1}	V _{BP} = 0 V, T _J = 25 °C	LNK454	-5.9	-4.2	-2.5	mA
			LNK456/457/458	-8.3	-5.9	-3.5	
			LNK460	-11.9	-8.5	-5.1	
	I _{CH2}	V _{BP} = 4 V, T _J = 25 °C	LNK454	-3.4	-2.4	-1.4	mA
			LNK456/457/458	-5.2	-3.7	-2.2	
			LNK460	-8.0	-5.7	-3.4	
BYPASS Pin Voltage	V _{BP}			5.60	5.85	6.15	V
Circuit Protection							
Current Limit	I _{LIMIT(MIN)}	di/dt = 160 mA/μs T _J = 25 °C	LNK454	245	264	283	mA
		di/dt = 325 mA/μs T _J = 25 °C	LNK456	491	528	565	
		di/dt = 490 mA/μs T _J = 25 °C	LNK457	790	850	910	
		di/dt = 650 mA/μs T _J = 25 °C	LNK458	1023	1100	1177	
		di/dt = 980 mA/μs T _J = 25 °C	LNK460	1581	1700	1819	
Leading Edge Blanking Time	t _{LEB}	T _J = 25 °C		160	200		ns
Current Limit Delay	t _{ILD}	T _J = 25 °C			150		ns
Thermal Shutdown Temperature	T _{SD}			135	142	150	°C
Thermal Shutdown Hysteresis	T _{SD(H)}				75		°C
BYPASS Pin Power-up Reset Threshold Voltage	V _{BP(RESET)}				4.9		V

Parameter	Symbol	Conditions SOURCE = 0 V; T _J = -40 to +125 °C (Unless Otherwise Specified)		Min	Typ	Max	Units
Output							
ON-State Resistance	R _{DS(ON)}	LNK454 I _D = 26 mA	T _J = 25 °C		23.1	26.6	Ω
			T _J = 100 °C		34.4	39.8	
		LNK456 I _D = 53 mA	T _J = 25 °C		11.7	13.5	
			T _J = 100 °C		17.5	20.2	
		LNK457 I _D = 85 mA	T _J = 25 °C		6.9	7.9	
			T _J = 100 °C		10.4	11.9	
		LNK458 I _D = 110 mA	T _J = 25 °C		4.4	5.1	
			T _J = 100 °C		6.7	7.6	
LNK460 I _D = 170 mA	T _J = 25 °C		2.2	2.6			
	T _J = 100 °C		3.3	3.9			
OFF-State Leakage	I _{DSS1}	V _{BP} = 6.2 V, V _{FB} > V _{FB(SK)} , V _{DS} = 580 V, T _J = 125 °C				50	μA
Breakdown Voltage	BV _{DSS}	V _{BP} = 6.2 V, V _{FB} > V _{FB(SK)} , T _J = 25 °C		725			V
DRAIN Supply Voltage				50			V
Auto-Restart OFF-Time	t _{AR(OFF)}	f _{MAIN} = 50 Hz			1.28		s
		f _{MAIN} = 60 Hz			1.02		
Auto-Restart Duty Cycle	DC _{AR}				33		%

Typical Performance Characteristics

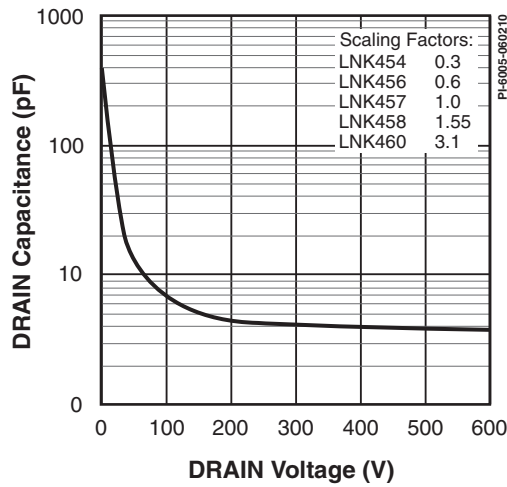


Figure 7. Drain Capacitance vs. Drain Voltage.

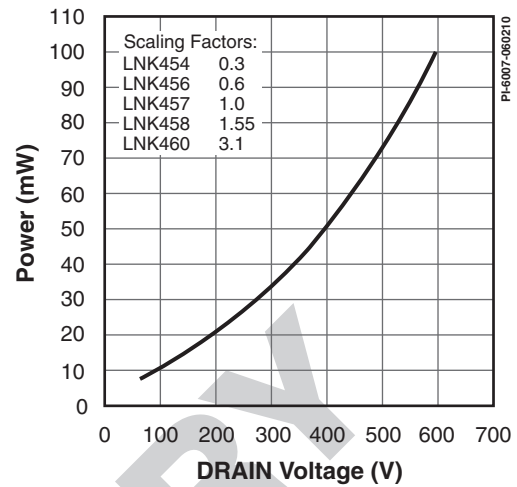


Figure 8. Power vs. Drain Voltage.

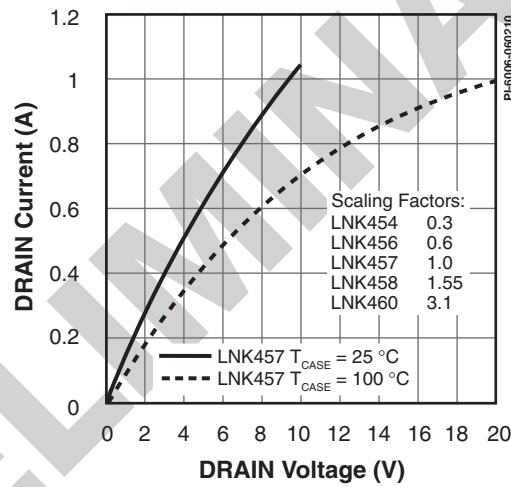
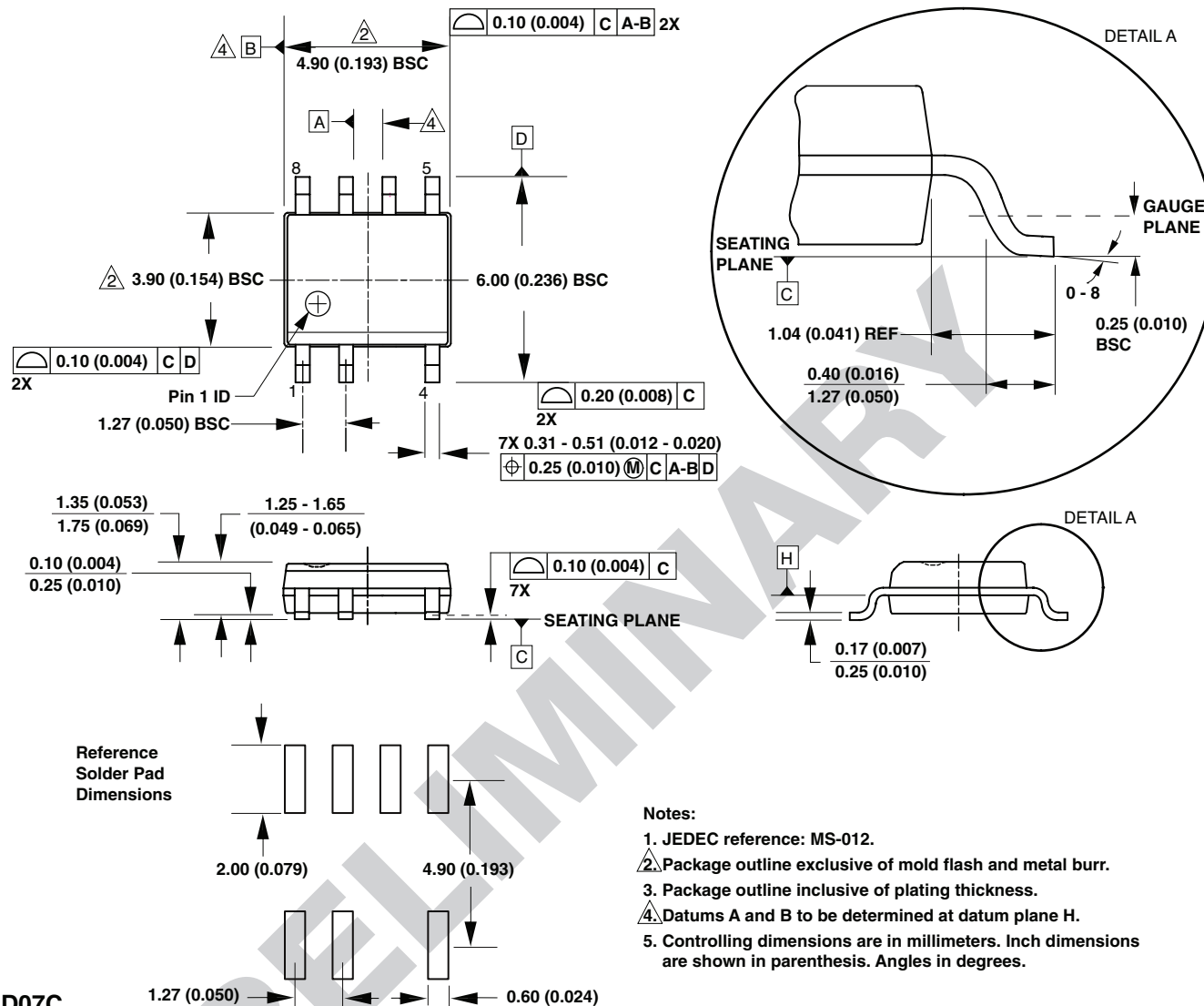
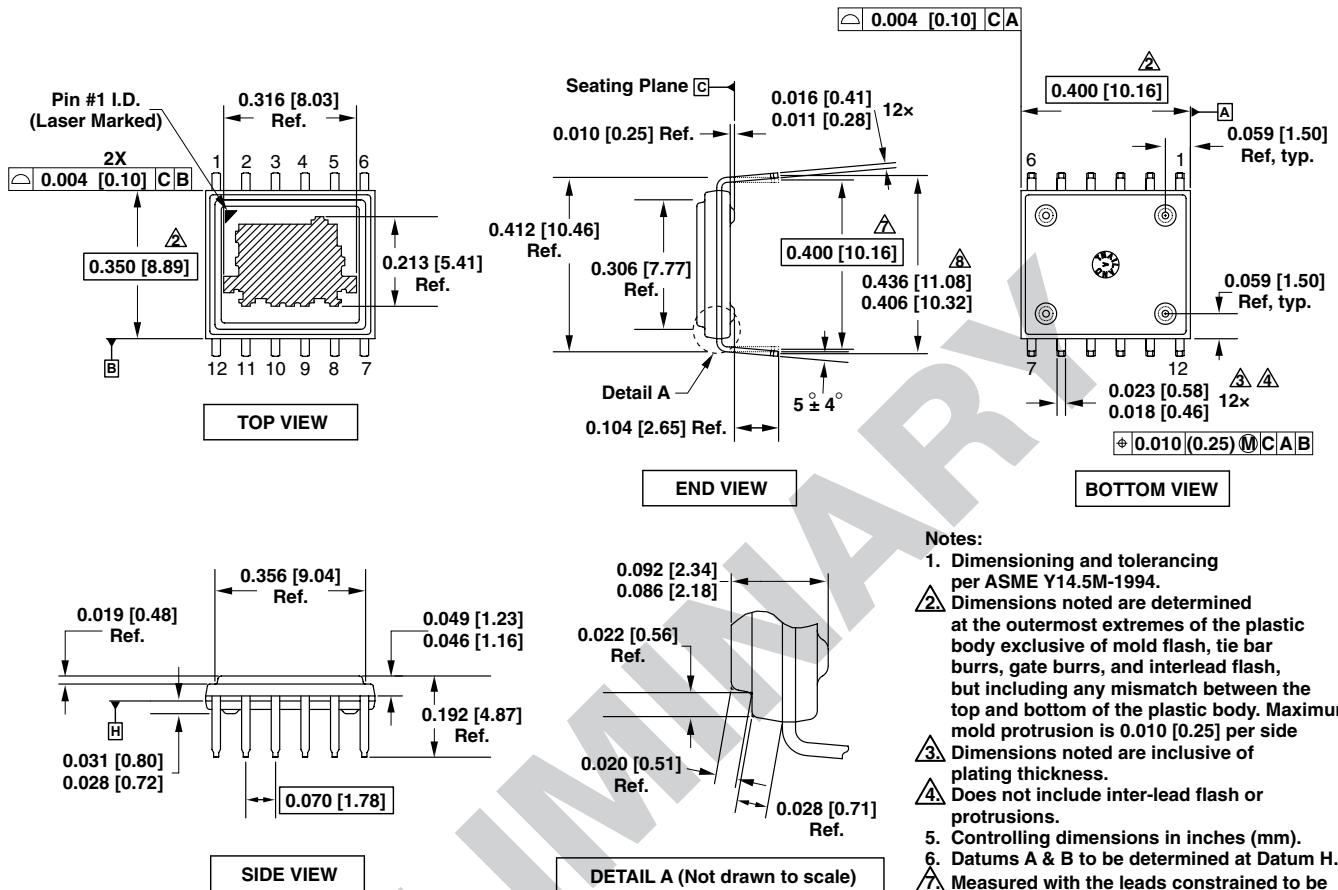


Figure 9. Drain Current vs. Drain Voltage.

SO-8C (D Package)



eDIP-12 (V Package)

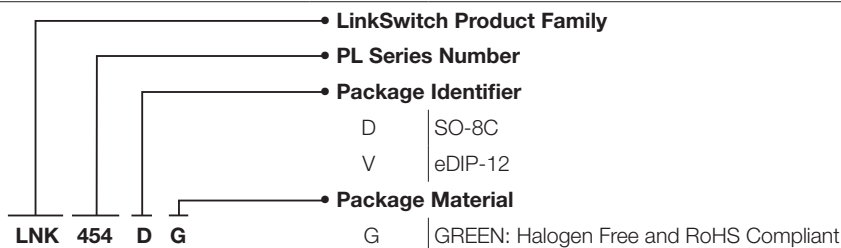


Notes:

1. Dimensioning and tolerancing per ASME Y14.5M-1994.
2. Dimensions noted are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs, and interlead flash, but including any mismatch between the top and bottom of the plastic body. Maximum mold protrusion is 0.010 [0.25] per side.
3. Dimensions noted are inclusive of plating thickness.
4. Does not include inter-lead flash or protrusions.
5. Controlling dimensions in inches (mm).
6. Datums A & B to be determined at Datum H.
7. Measured with the leads constrained to be perpendicular to Datum C.
8. Measured with the leads unconstrained.
9. Lead numbering per JEDEC SPP-012.

PI-5556-051010

Part Ordering Information



Revision	Notes	Date
A	Preliminary Release	06/09/10

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